identifying numeral. FIG. **2** shows that the trenches, for example, trench **49** of FIG. **1** can be lined with a high resistivity material, for example, silicon dioxide layers **60** and **61** before filling with SIPOS filler **48** (or polysilicon) to further reduce leakage current. Care should be taken to ensure that all P diffusions are suitably connected together when using the embodiment of FIG. **2**.

FIG. **3** shows a termination structure which can be used for the chip **10**, using the same process steps used in Figures and **2** for the formation of trenches **49**, **50** and **51**. Thus, in the termination region, further P diffusions **70** and **71** are formed, but no source is formed in these termination diffusions (which may encircle the chip). Trenches **75** and **76** and other concentric trenches bisect their respective bases **70** and **71** and are lined with SiO_2 layers and are filled with SIPOS or polysilicon fillers **77** and **78** respectively. Spaced conductive rings **79** and **80**, which float relative to source **39**, contact P regions **70** and **71** and fillers **77** and **78** respectively. Thus, the epi regions **12** between trenches **75** and **76** and regions on opposite sides of these trenches deplete during blocking or reverse voltage conditions.

Although the present invention has been described in relation to particular embodiments thereof, many other variations and modifications and other uses will become apparent to those skilled in the art. It is preferred, therefore, that the present invention be limited not by the specific disclosure herein, but only by the appended claims.

What is claimed is:

1. A high voltage MOSgated device of low on-resistance comprising, in combination; a thin flat chip of silicon having a main body layer of one conductivity type and having relatively high concentration and a junction-receiving layer of said one conductivity type and of a relatively lower concentration disposed atop said main body layer; a plurality of spaced base diffusions of the other conductivity type formed in the upper surface of said junction receiving layer and a plurality of source regions of said one conductivity type formed in respective ones of said base diffusions to define invertable channel regions laterally spaced from one another by a vertical conduction channel region in said junction receiving layer; and a MOSgate structure disposed above each of said invertible channels and responsive to a suitable MOSgate input signal; a plurality of spaced thin trenches extending vertically from the top of said junction receiving layer for at least a major portion of the thickness of said junction receiving layer; a first main contact disposed above the top surface of said junction receiving layer and in contact with said source and base diffusions and said trenches; a second main contact formed on the bottom of said main body layer; said trenches defining between them vertical depletable vertical conduction regions in said junction receiving layer for the length of said trenches; each of said trenches being filled with a semi-insulating, non-injecting material which is relatively incapable of carrier injection into the junction receiving layer.

2. The device of claim, **1** wherein said semi-insulating material comprises a SIPOS semi-insulating polysilicon.

3. The device of claim **1**, wherein said trenches are lined with silicon dioxide and are filled with polysilicon.

4. The device of claim **1**, wherein said trenches have a depth which reaches said body layer.

5. The device of claim **2**, wherein said trenches have a depth which reaches said body layer.

6. The device of claim **3**, wherein said trenches have a depth which reaches said body layer.

7. The device of claim **1** wherein said trenches have a width of about 1 micron.

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